REMARKS

The Office Action dated March 6, 2006 in this Application has been carefully considered. Claims 1-3, 6-9, 12-15, and 19-24 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-3, 7-9, 13-15, and 19 have been amended in this Response. Claims 4, 5, 10, 11, 16, and 17 have been cancelled in this Response. Claims 21-24 are new and have been added in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

The Specification stands objected to because of an identified informality. Applicants have amended the Specification to address the identified informality and other minor typographical errors. Accordingly, Applicants respectfully request that the objection to the Specification be withdrawn.

Claims 1-20 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 6,615,380 B1 by Kapur et al. ("Kapur") in view of U.S. Patent No. 6,766,487 B2 by Saxena et al. ("Saxena"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claims 1, 13, and 19, Kapur was cited as assertedly fully disclosing, "a electronics design automation (EDA) system for designing integrated circuits (IC) with design for test (DFT) technique and test synthesis tool and method including computer program product for configuration circuitry for partitioning at least one scan chain into a plurality (multiple) of segments and enables each segment to be selectively bypassed or deactivated during the test application." Office Action, at Page 3 (*citing* Kapur, col. 1, lines 7-10, 23-40; col. 2, lines 17-28; and col. 4, lines 26-34).

The Examiner admits that "Kapur does not teach explicitly scanning one of the plurality of segments at a time." Office Action, at Page 3. Saxena, however, was cited as assertedly fully disclosing, "a low power scan architecture (scan circuitry) . . . including a processor (core) having one or more scan chains with multiple segments (fig. 20) and method for scanning including scanning one of the plurality of segments at a time." Office Action, at Page 3 (*citing* Saxena, col. 3, lines 35-55; col. 4, lines 43-67; col. 5, lines 17-52; col. 11, lines 47-67; col. 12, lines 1-30; col. 13, lines 32-57; col. 15. lines 9-67; col. 16, lines 1-46).

The Examiner further stated that it would have been obvious to combine the teachings of Kapur and Saxena "to modify the EDA system, DFT technique and a test synthesis tool to include scanning (testing) of each circuit (segment) at a time as taught by Saxena in order to obtain an improved test synthesis tool to provide direct synthesis of low power scan architecture and eliminate the need to perform the adaptation steps." Office Action, at Page 3 (*citing* Saxena, col. 12, lines 25-40).

First, Applicants note that Claims 4, 5, 10, 11, 16, and 17 have been cancelled in this Response. As such, Applicants submit that the rejections as to Claims 4, 5, 10, 11, 16, and 17 are moot.

Second, rejected independent Claims 1, 7, 13, and 19 as now amended more particularly recite one of the distinguishing characteristics of the present invention, namely, "partitioning at least one scan chain into a plurality of segments *comprising one or more segments of a predetermined length and an offset segment,*" "*providing enough clocking to scan all bits in the plurality of segments,*" "keeping track of" or "tracking," "*the predetermined length, an order of the segments, and the offset segment,*" and "scanning *all* of the plurality of segments *one segment* at a time."

(Emphasis added.) Support for these Amendments can be found, among other places, at Page 4, lines 15-24 and at Page 11, line 26 through Page 12, line 6 of the original Application.

Neither Kapur nor Saxena individually or in combination suggest, teach, or disclose "partitioning at least one scan chain into a plurality of segments comprising one or more segments of a predetermined length and an offset segment," and "scanning *all* of the plurality of segments *one segment* at a time." Specifically, Kapur provides the ability to selectively bypass certain segments of a longer scan chain during testing. As such, the Kapur approach is expressly designed to "generat[e] test patterns such that test data volume and test data application time are significantly reduced." Kapur, col. 2, lines 12-15.

In particular, Kapur states:

> Since the purpose of a scan chain is to apply the test pattern, the present invention recognizes that the ideal scan chain for a pattern is one that includes *only* the scan cells specified in the test pattern. Approximately, for 90% of the test patterns, only 10% of the scan cells of the scan chain are needed. However, these 10% of the scan cells are never the same ones. The present invention recognizes that each test pattern should have its own scan chain and that test data volume can be significantly reduced if every test pattern is applied by its own scan chain.

Kapur, Col. 7, lines 1-9 (emphasis added).

But the unique invention described in the amended Claims partitions the "at least one scan chain into a plurality of segments comprising one or more segments of a predetermined length and an offset segment," and scans "*all* of the plurality of segments one segment at a time." Because the claimed invention is, for example, "A method for reducing scan power consumption *when unloading and restoring content of a processor* having one or more scan chains" as recited in Claim 1 (emphasis added), the claimed invention focuses on storing/loading the bit state of each and every bit in the scan chain. As such, the claimed invention includes all of the plurality of segments of the

at least one scan chain. By contrast, Kapur is expressly configured to optimize a test pattern by selectively *bypassing* one or more segments in a scan chain.

Accordingly, even assuming, *arguendo*, that there is some motivation to apply the teachings of Saxena as described by the Examiner to the Kapur system, a fact Applicants respectfully traverse, the proposed combination fails to teach each and every element as recited in the Claims. For at least this reason, the Examiner's proposed combination is insufficient to reject the Claims, as amended.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combinations now recited in amended Claims 1, 7, 13, and 19. Applicants therefore submit that amended Claims 1, 7, 13, and 19 are clearly and precisely distinguishable over the cited references in a patentable sense, and are therefore allowable over these references and the remaining references of record. Accordingly, Applicants respectfully request that the rejections of amended Claims 1, 7, 13, and 19 under 35 U.S.C. § 103(a) be withdrawn and that Claims 1, 7, 13, and 19 be allowed.

Claims 2, 3, and 6 depend on and further limit Claim 1. Claims 8, 9, and 12 depend on and further limit Claim 7. Claims 14, 15, and 18 depend on and further limit Claim 13. Claim 20 depends on and further limits Claim 19. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of the dependent Claims 2-3, 6, 8-9, 12, 14-15, 18, and 20 also be withdrawn and that dependent Claims 2-3, 6, 8-9, 12, 14-15, 18, and 20 be allowed.

New Claim 21 depends on and further limits Claim 1. New Claim 22 depends on and further limits Claim 7. New Claim 23 depends on and further limits Claim 13. New Claim 24 depends on and further limits Claim 19. Applicants respectfully submit that for at least the

aforementioned reasons, these Claims would also be deemed to be in condition for allowance. Applicants therefore respectfully request that new Claims 21-24 also be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-3, 6-9, 12-15, and 19-24.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 6/6/06

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